

FIG. 1

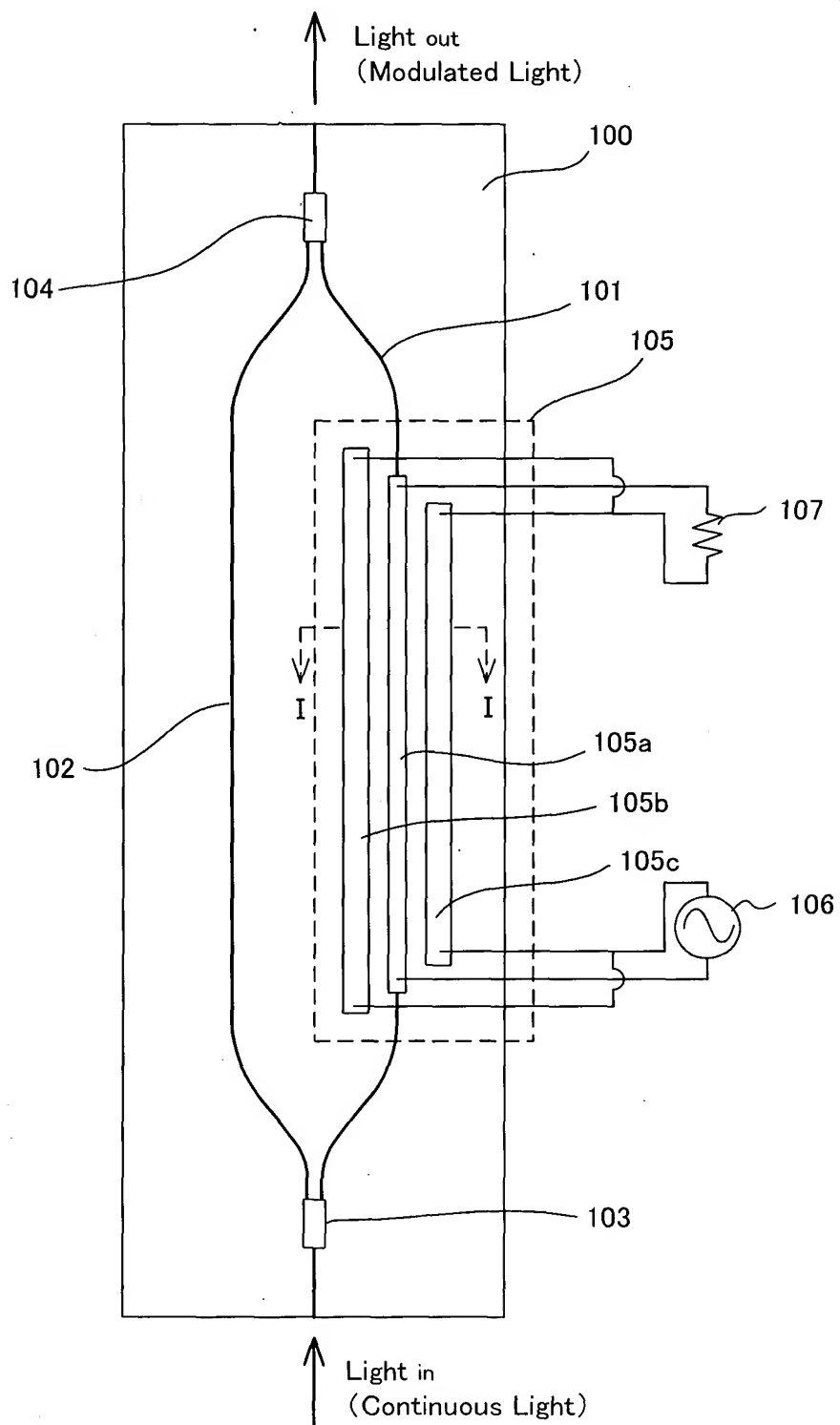


FIG. 2

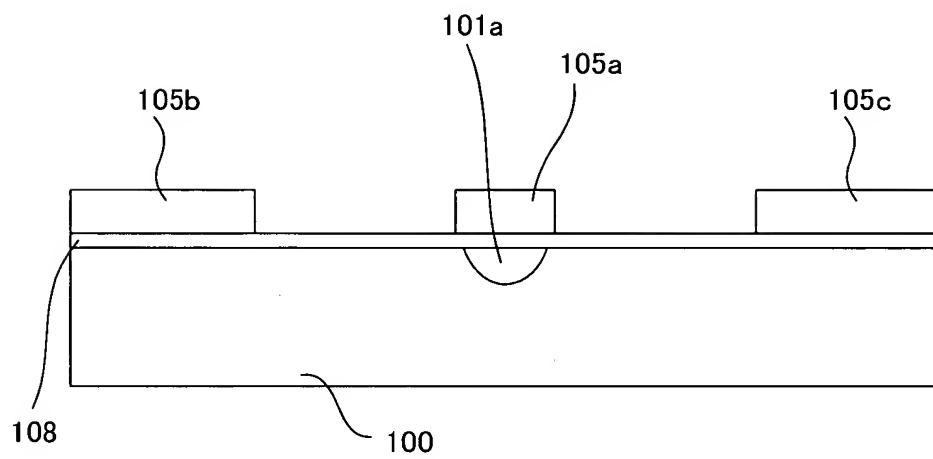


FIG. 3

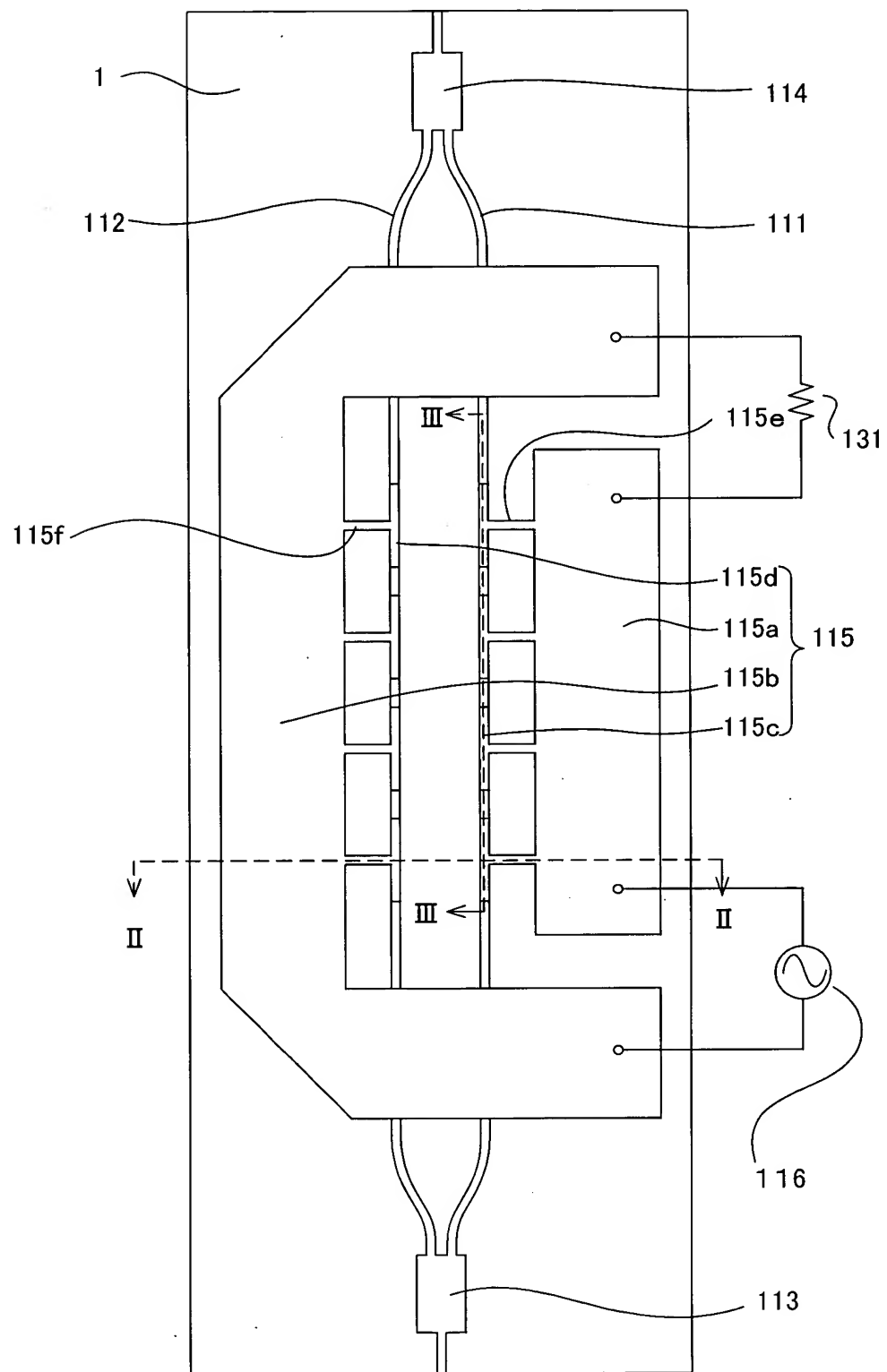


FIG. 4

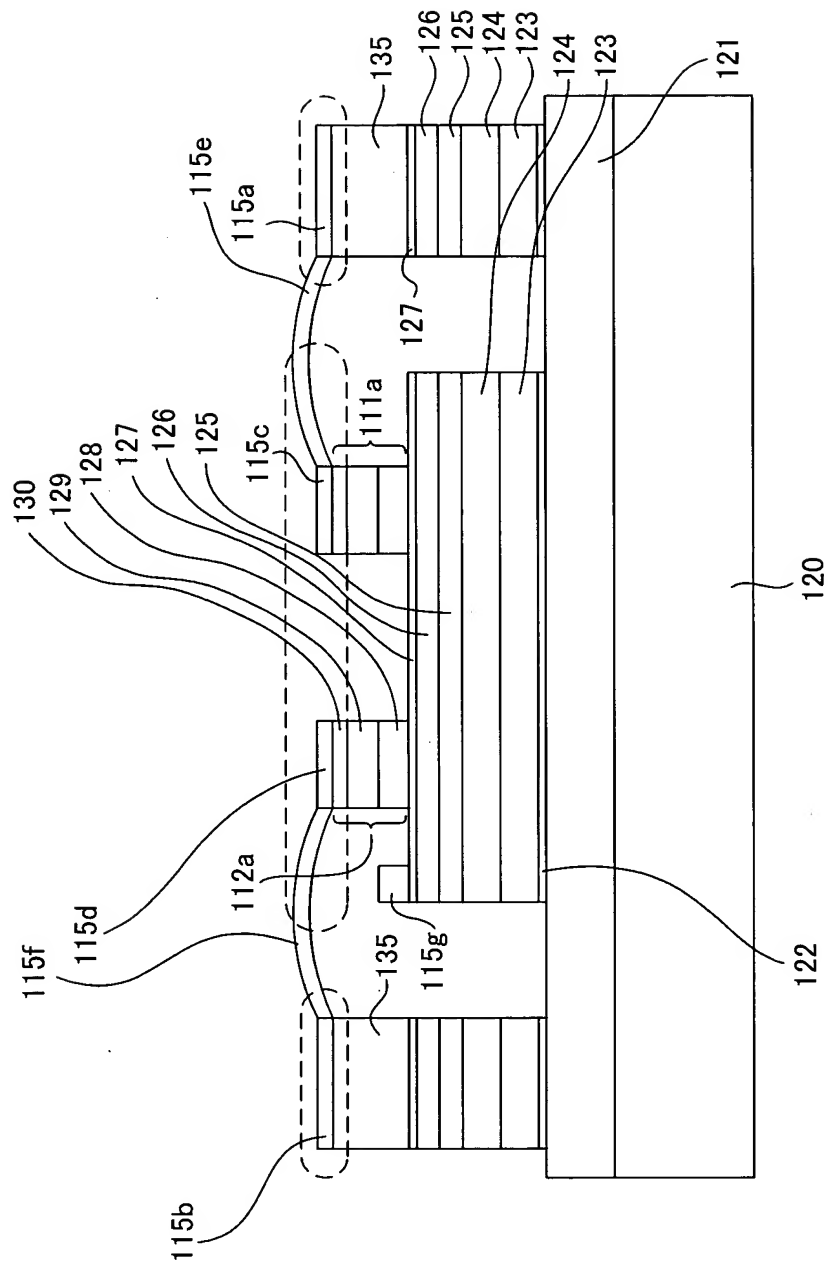


FIG. 5

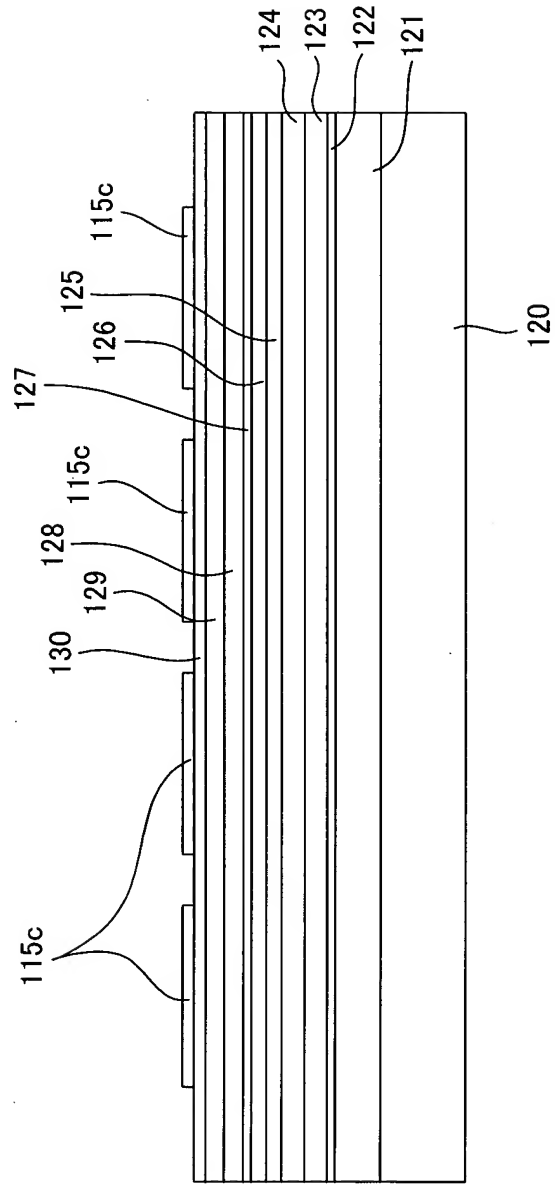


FIG. 6

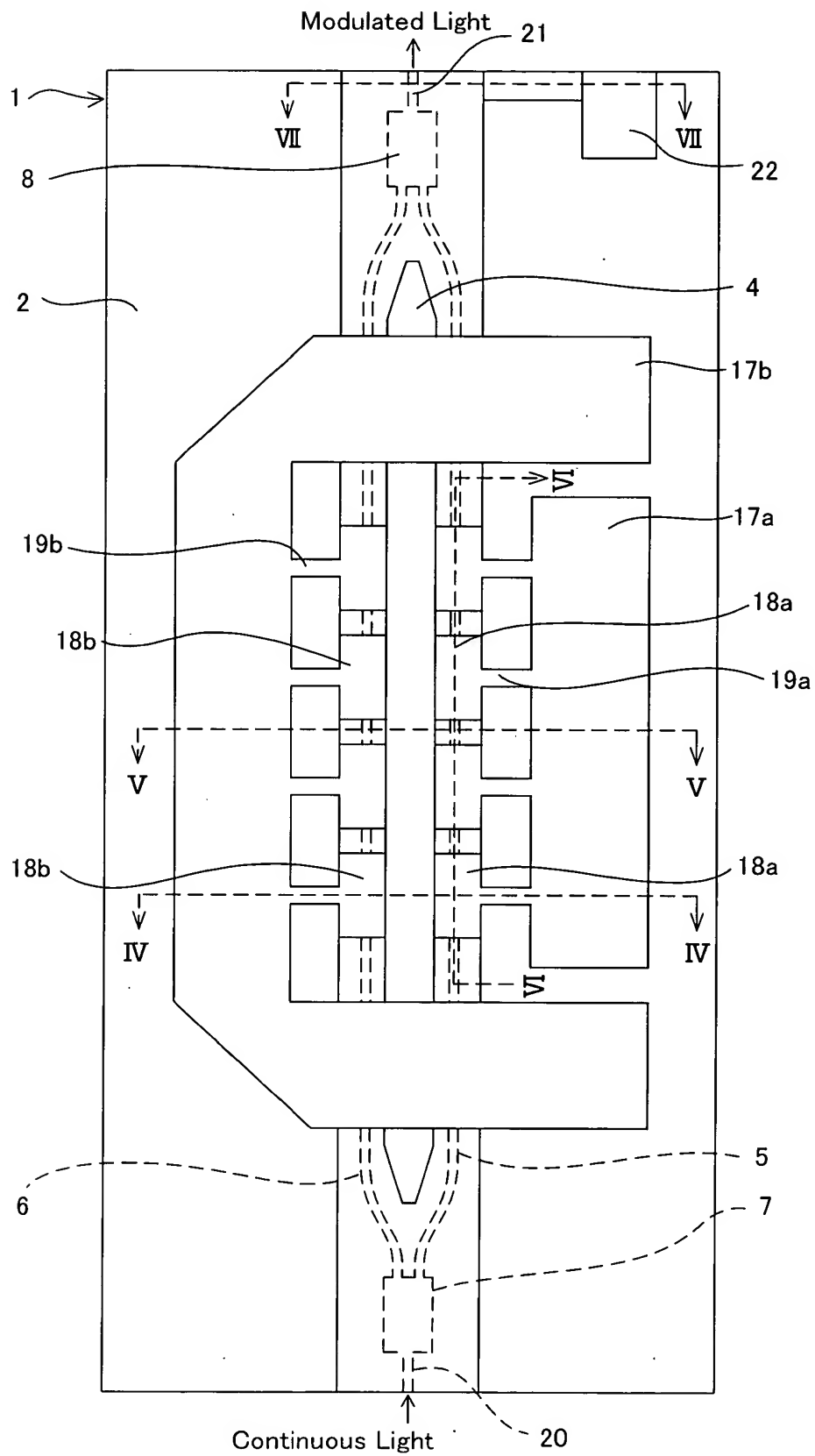


FIG. 7

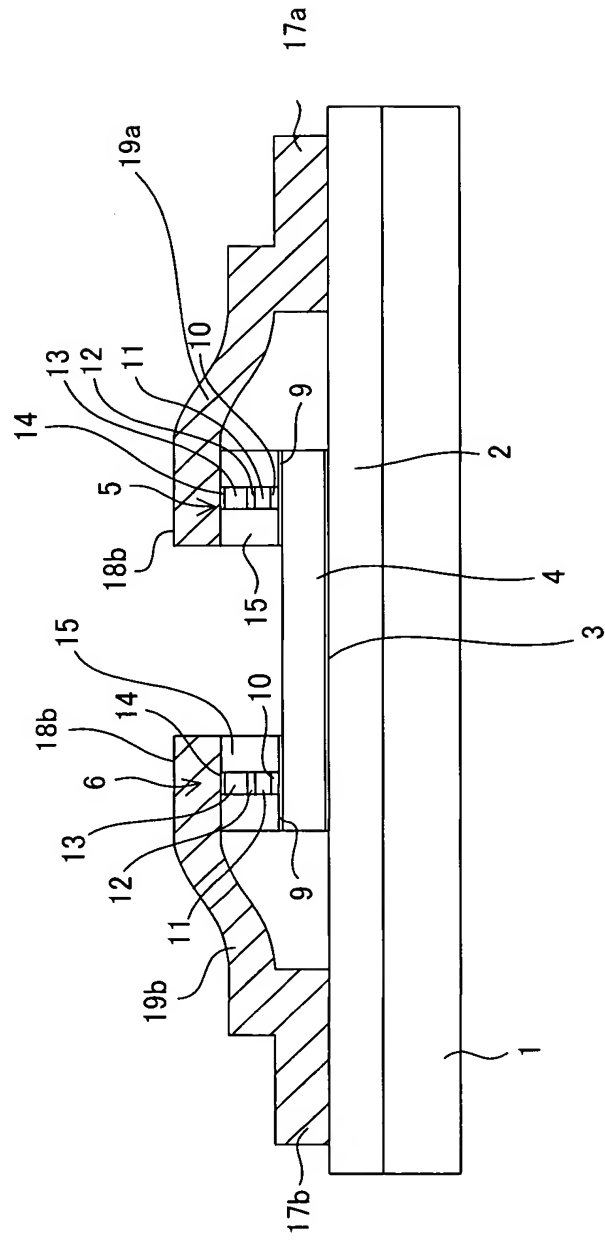


FIG. 8

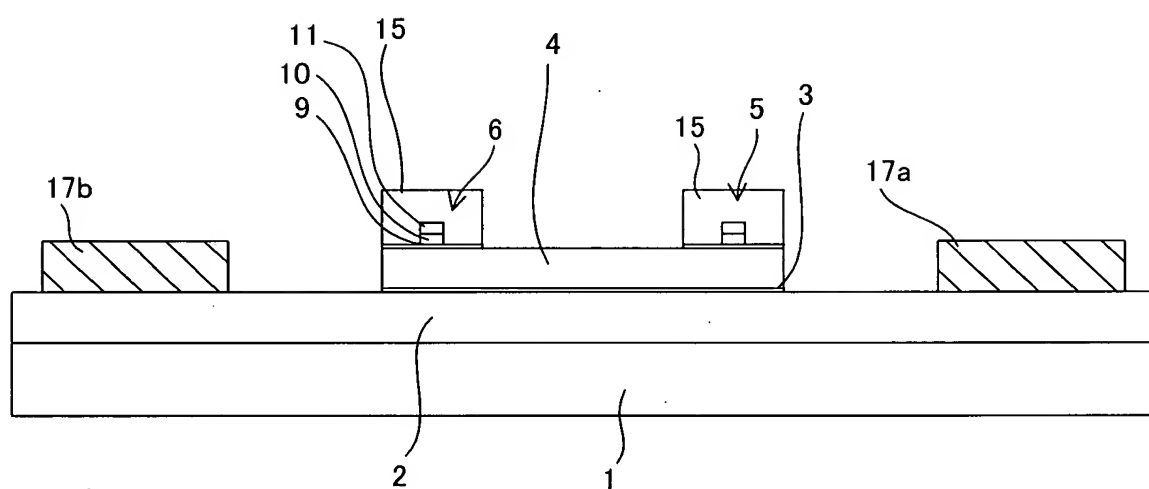




FIG. 9

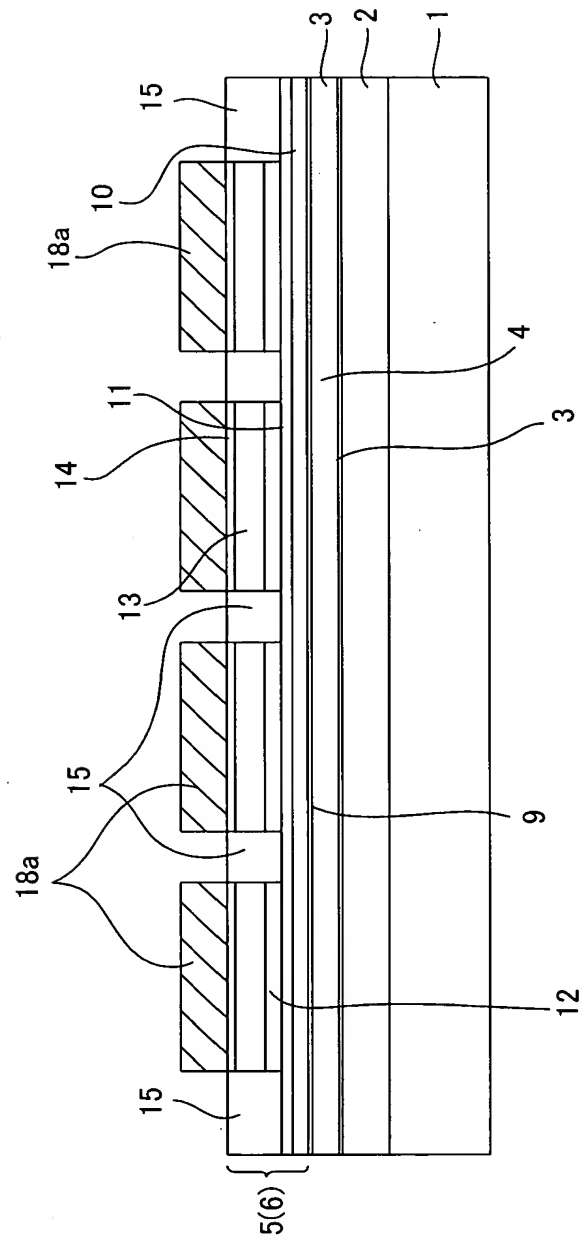


FIG. 10

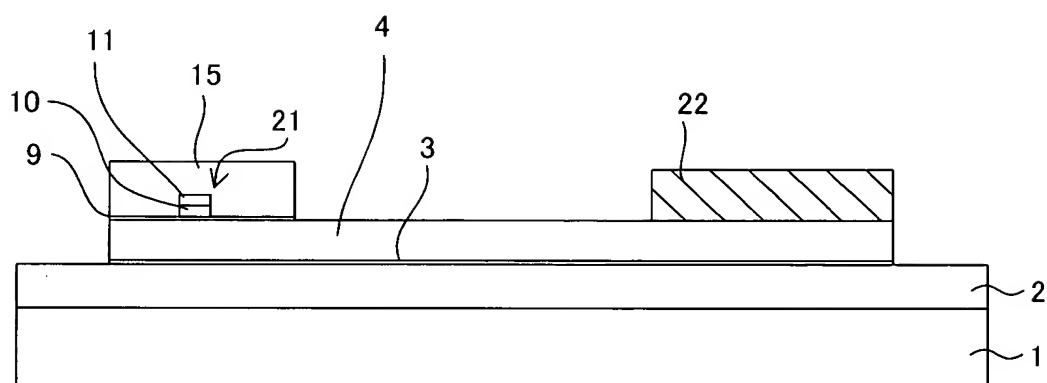


FIG. 11

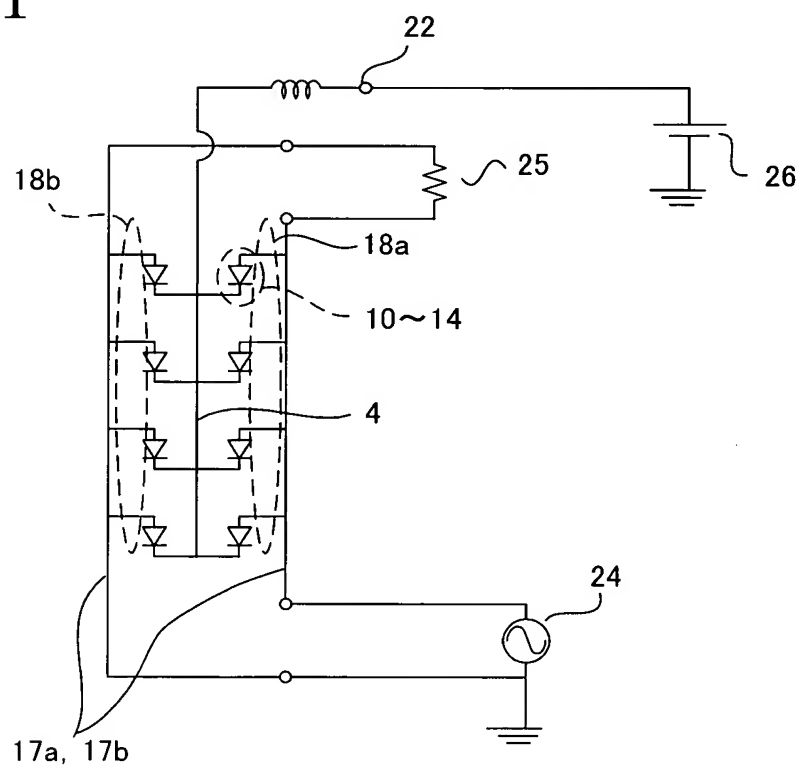


FIG. 12

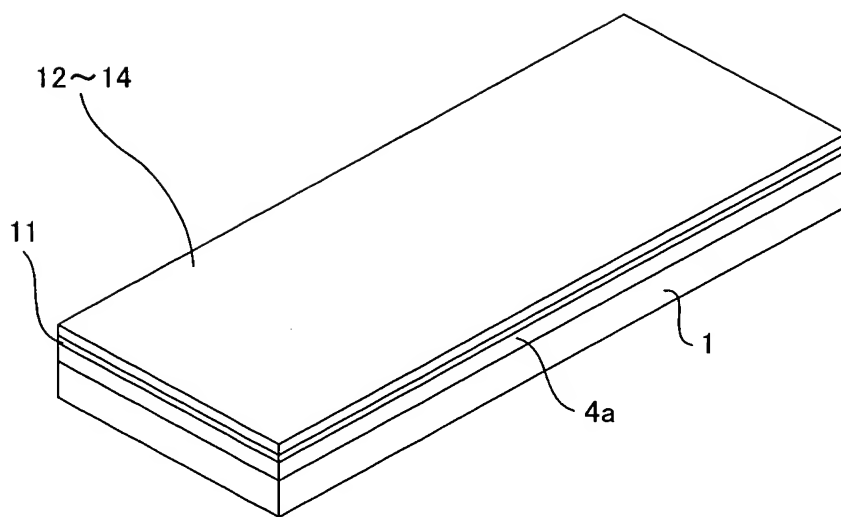


FIG. 13

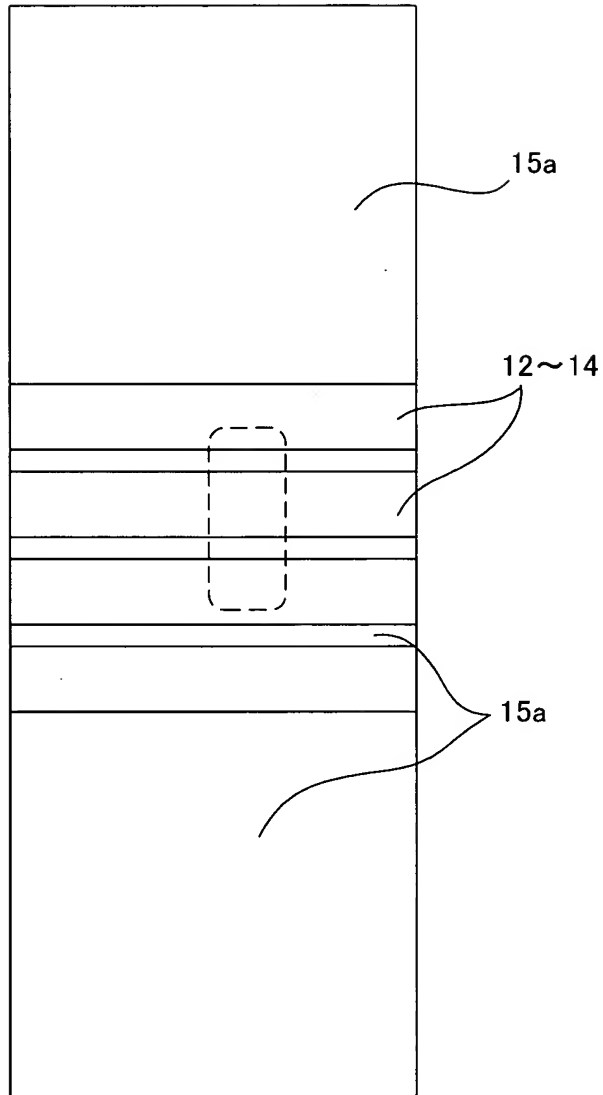


FIG. 14

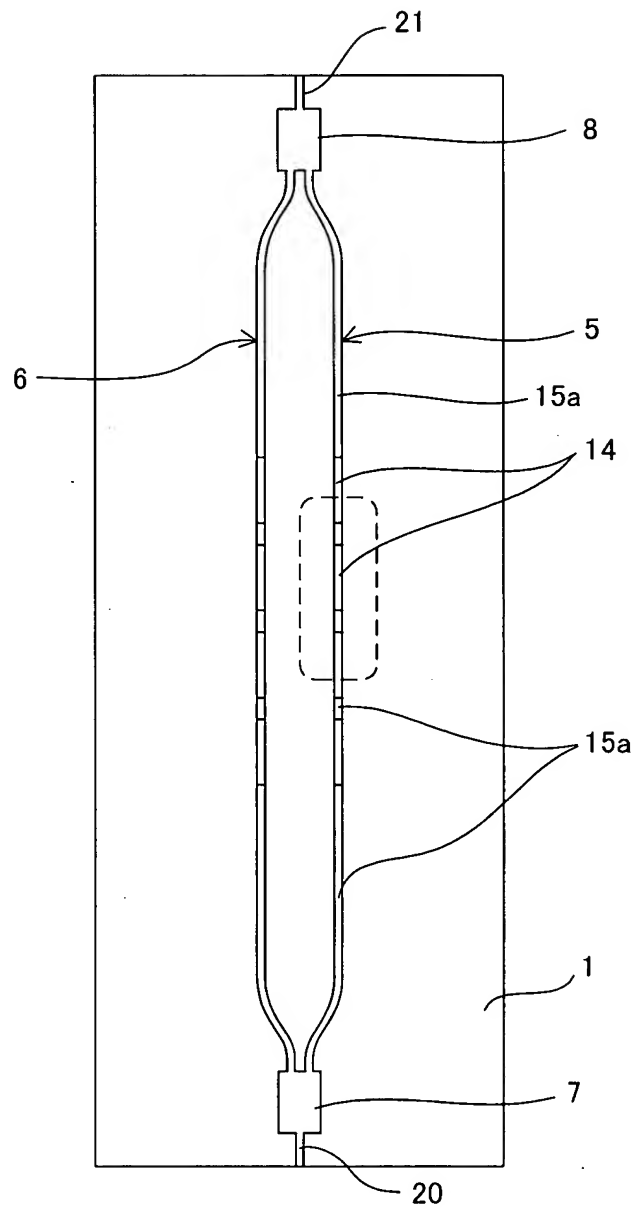


FIG. 15

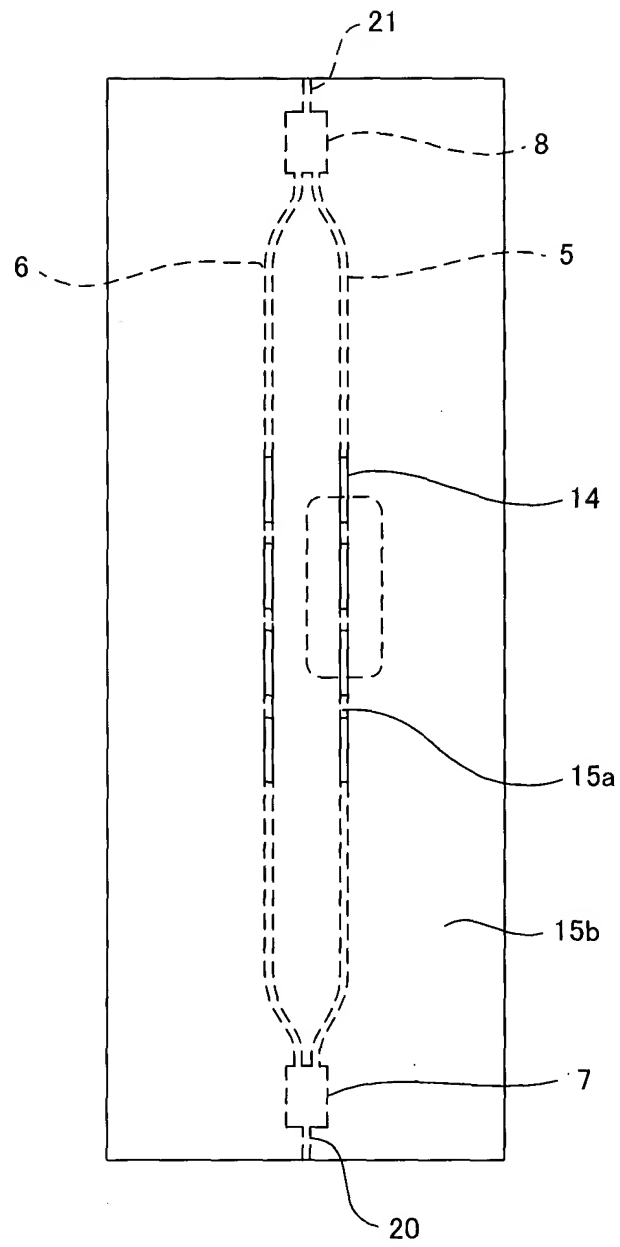


FIG. 16

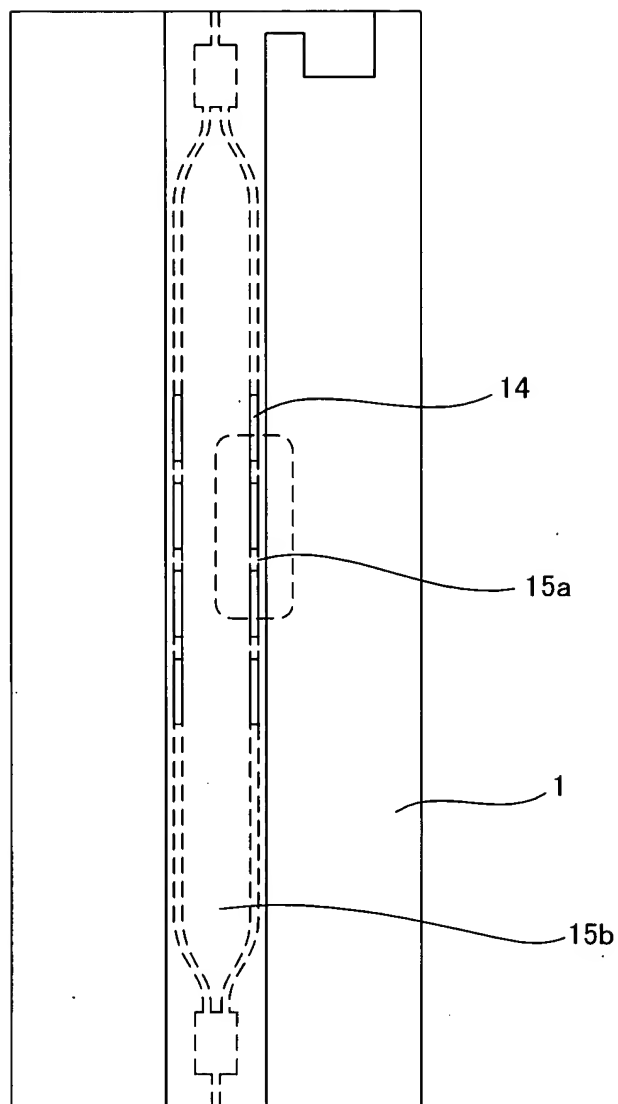


FIG. 17

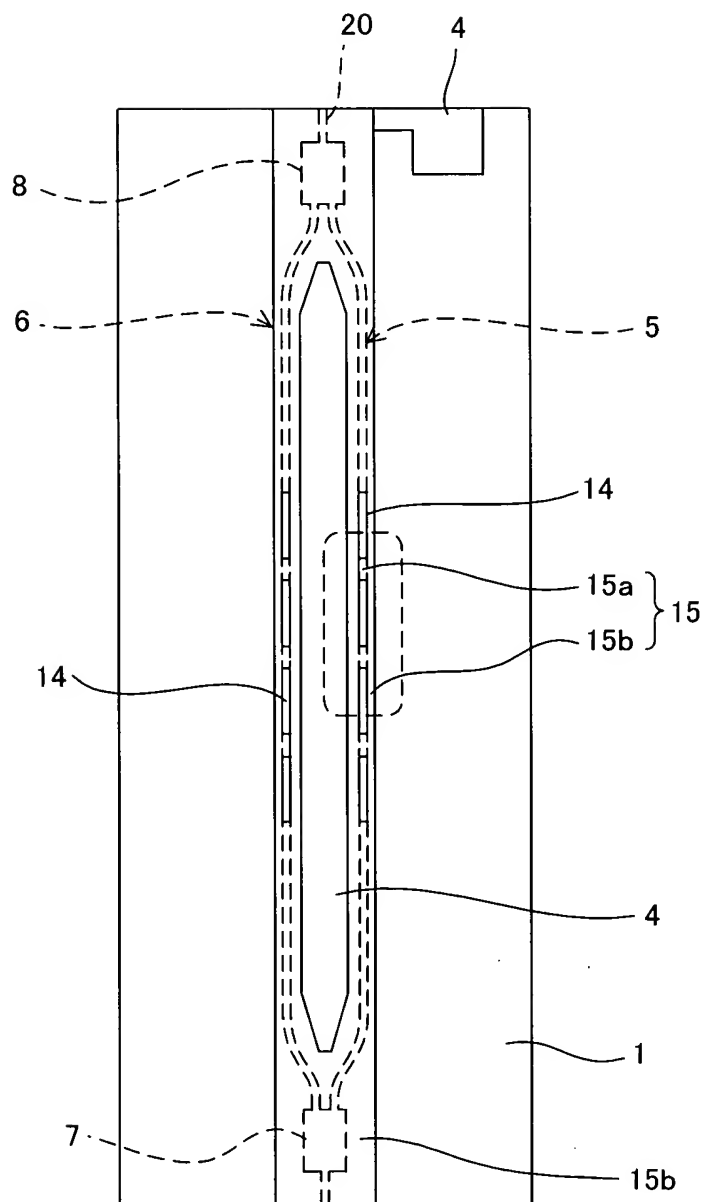




FIG. 18

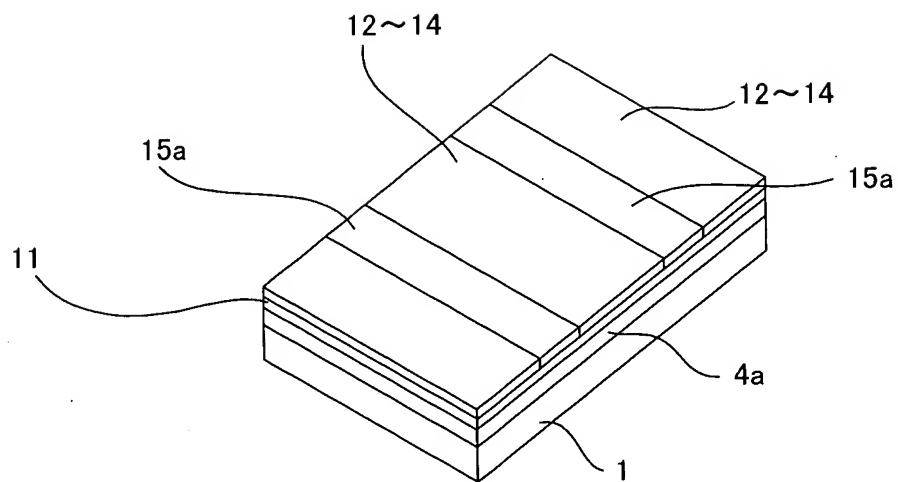


FIG. 19

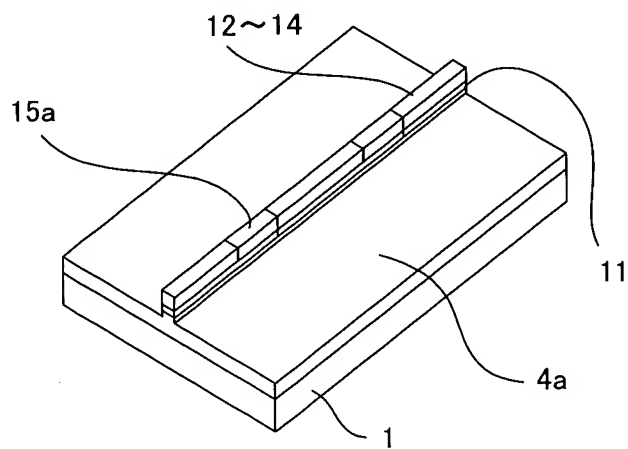


FIG. 20

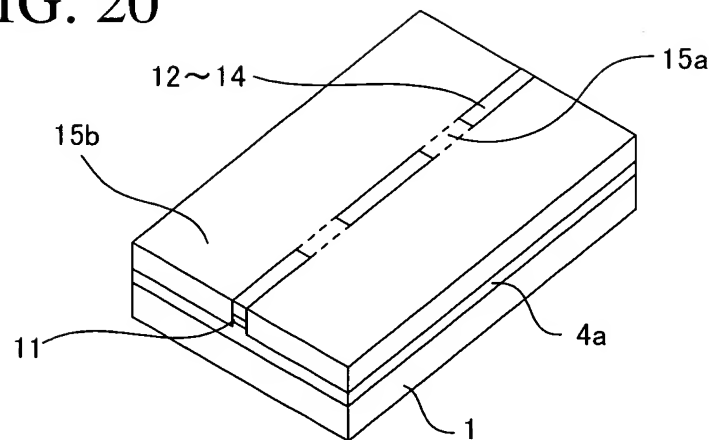


FIG. 21

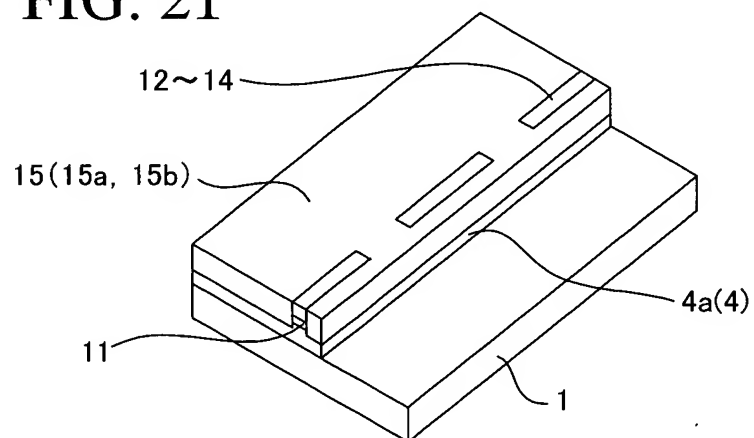


FIG. 22

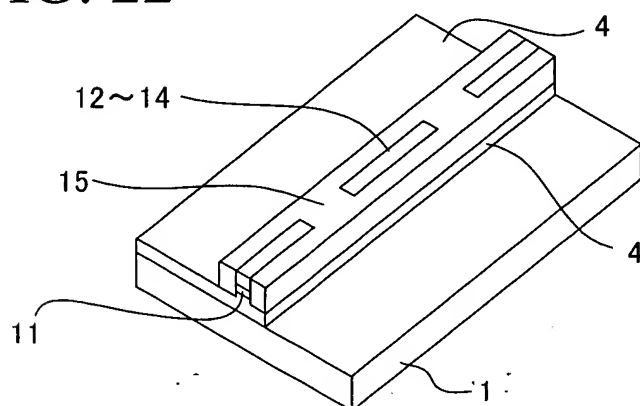


FIG. 23

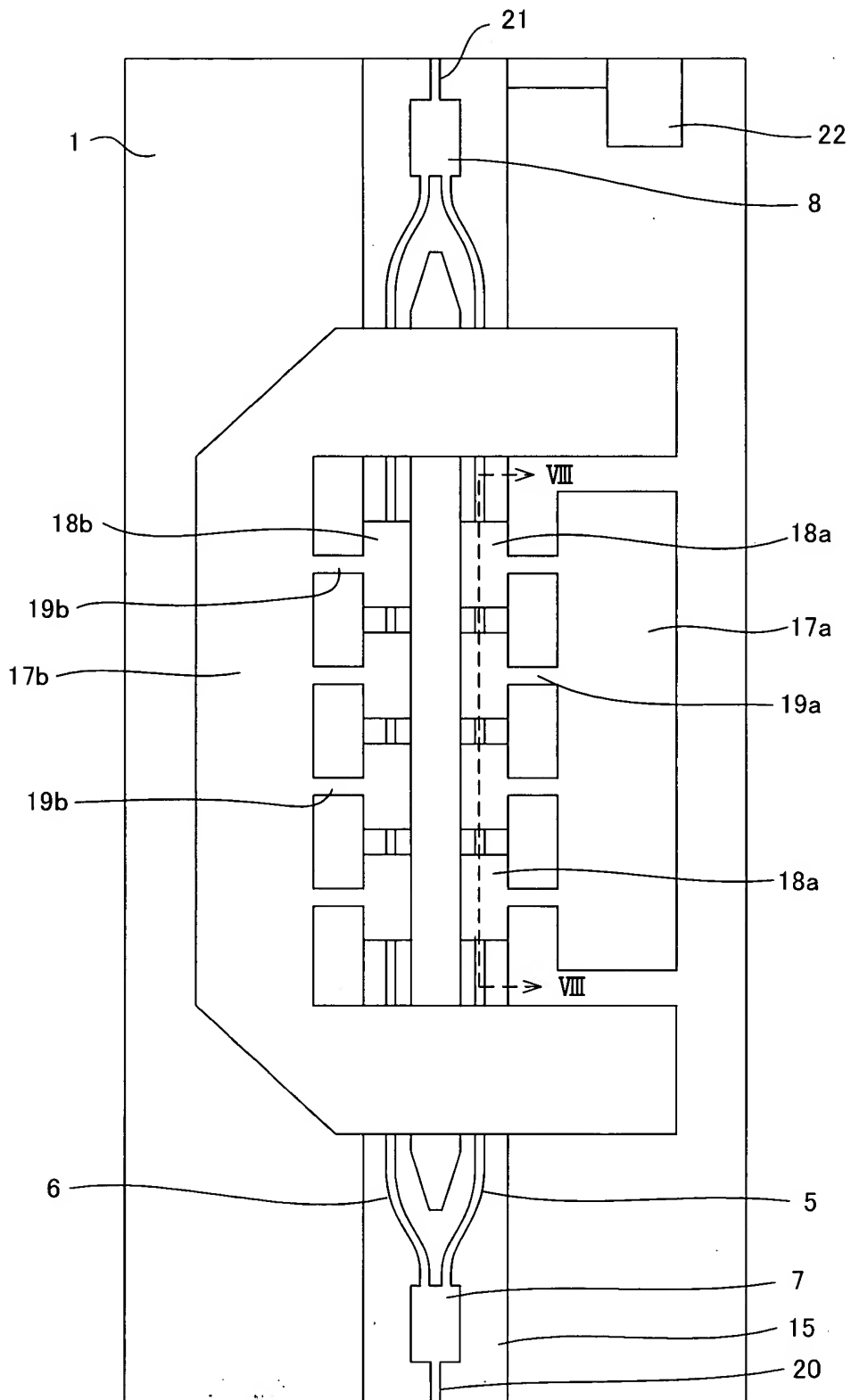


FIG. 24

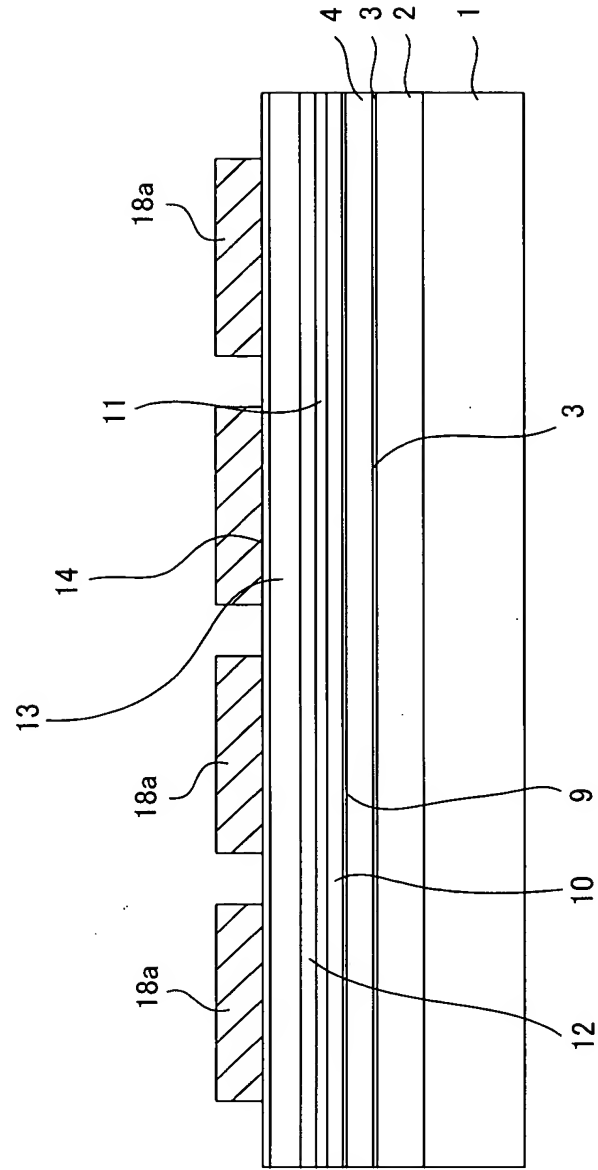


FIG. 25

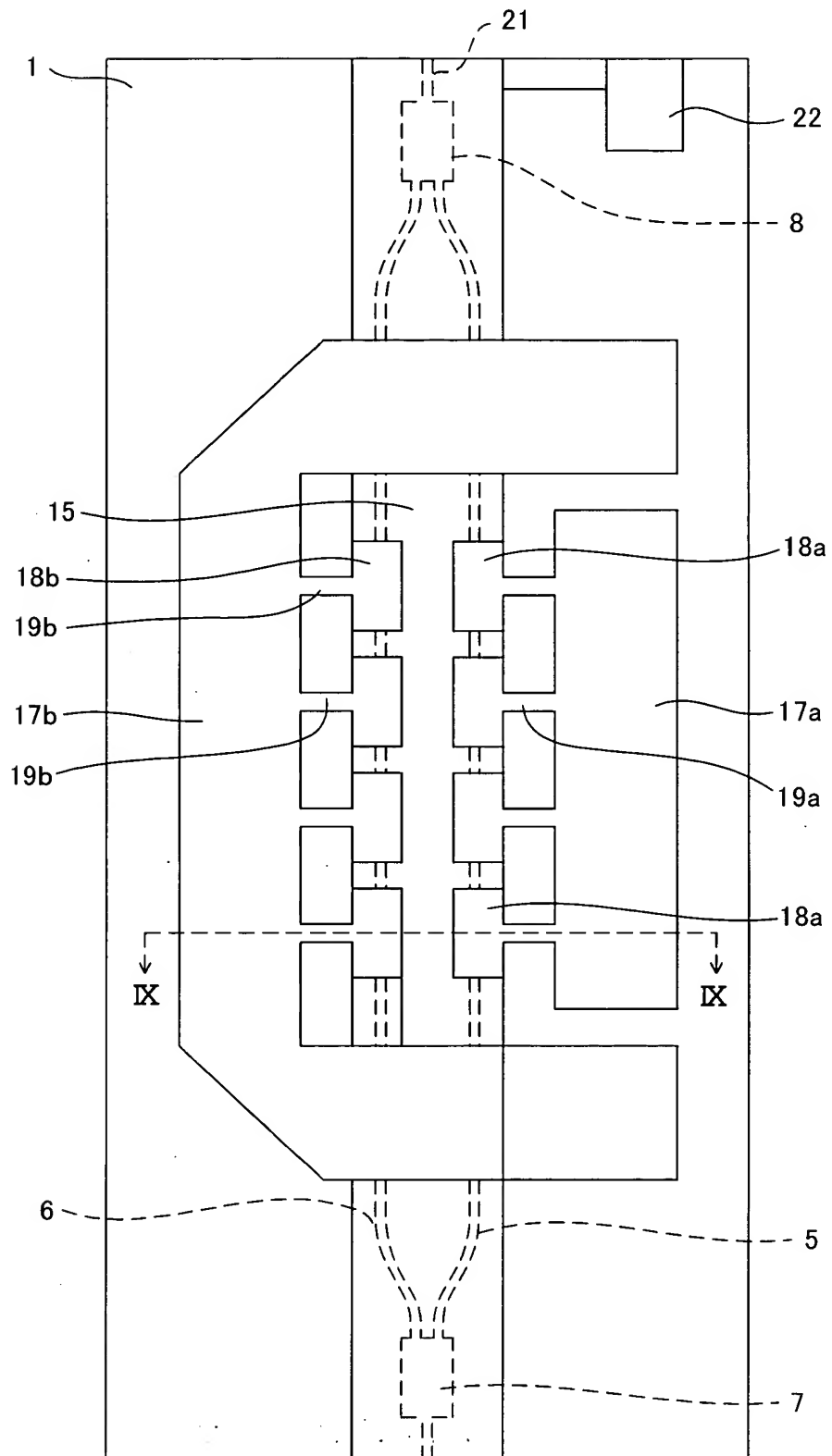
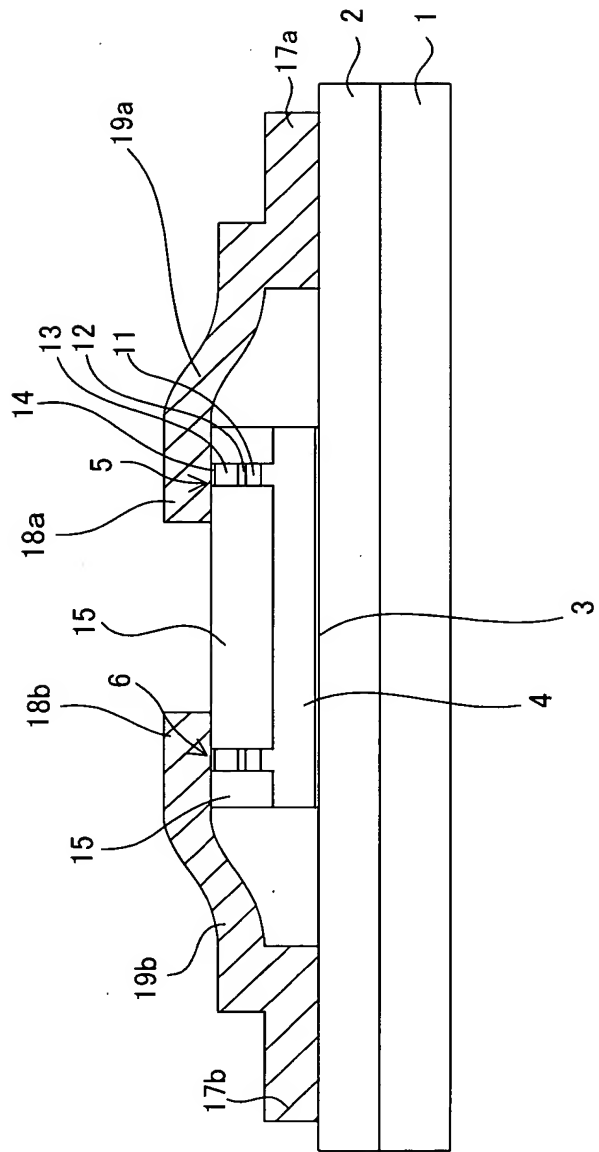


FIG. 26



# FIG. 27

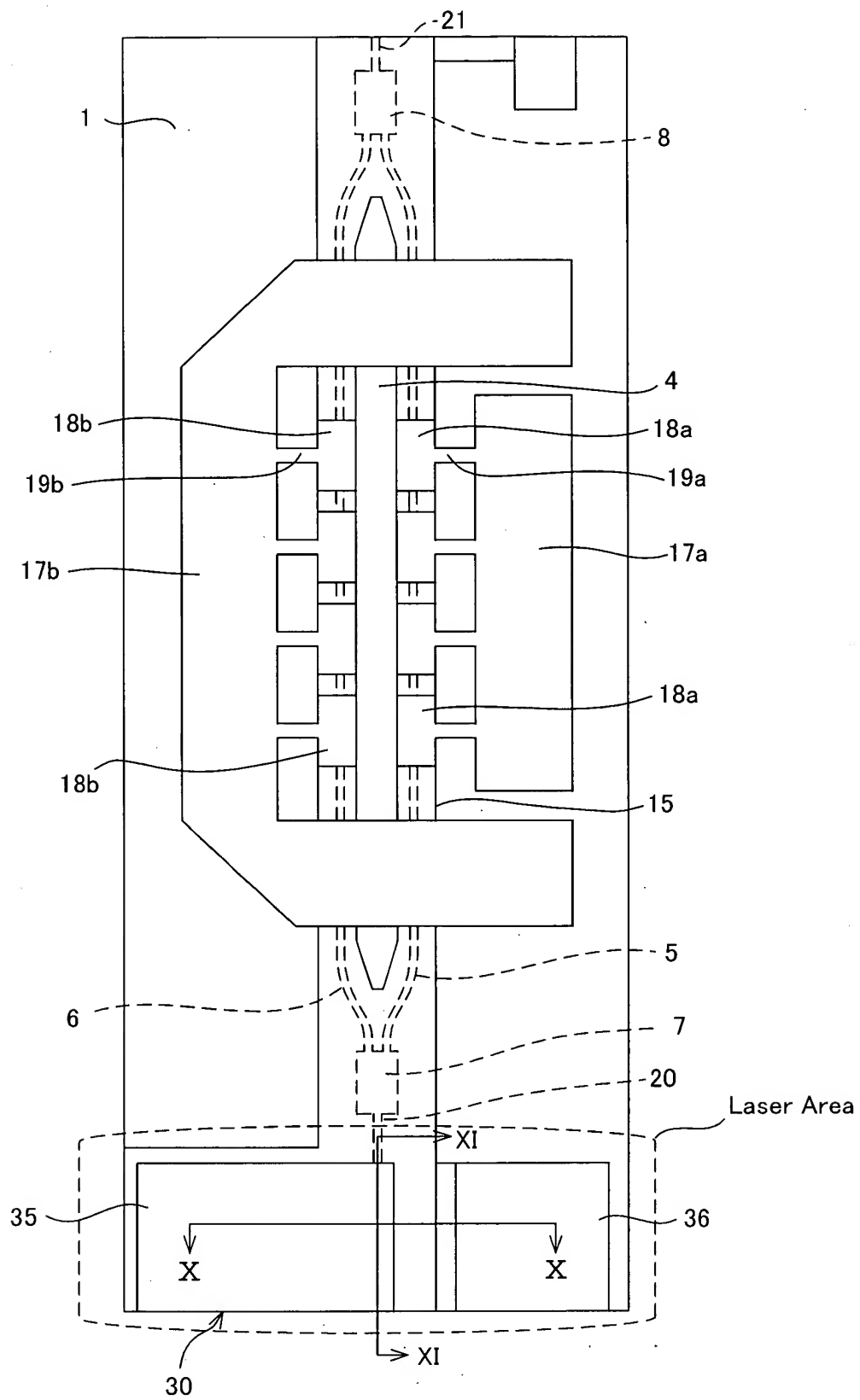


FIG. 28

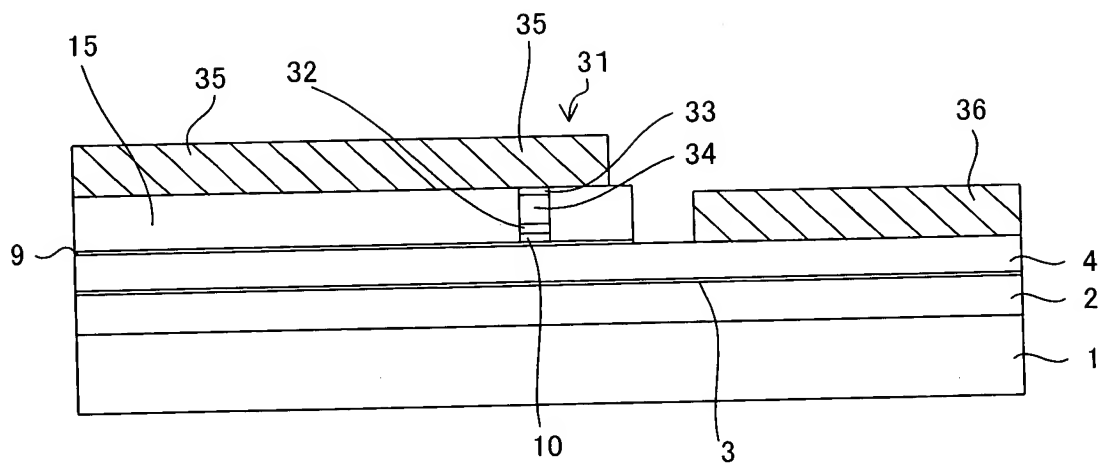


FIG. 29

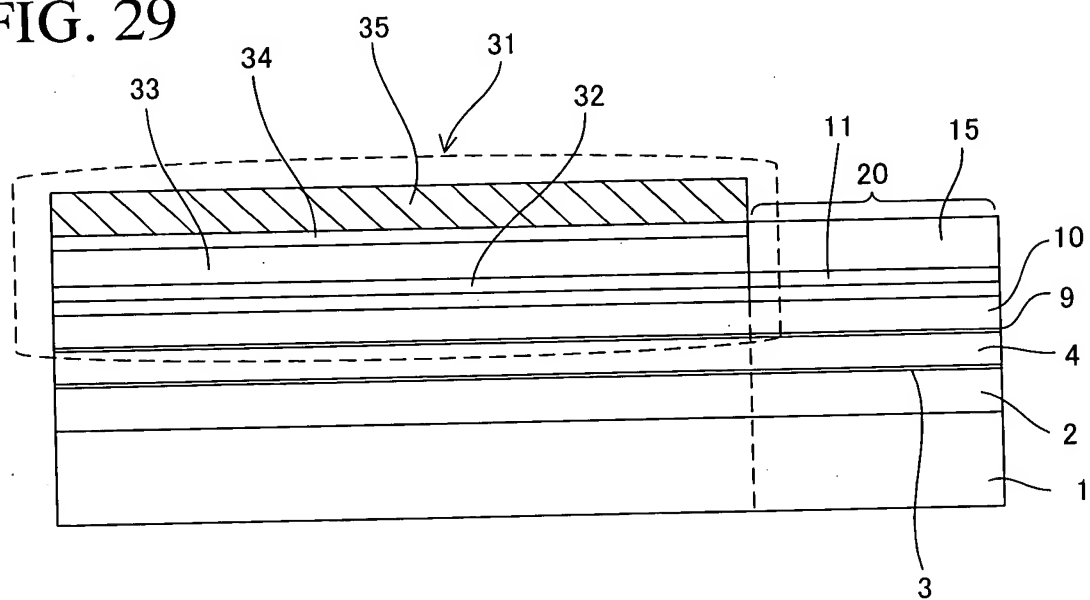
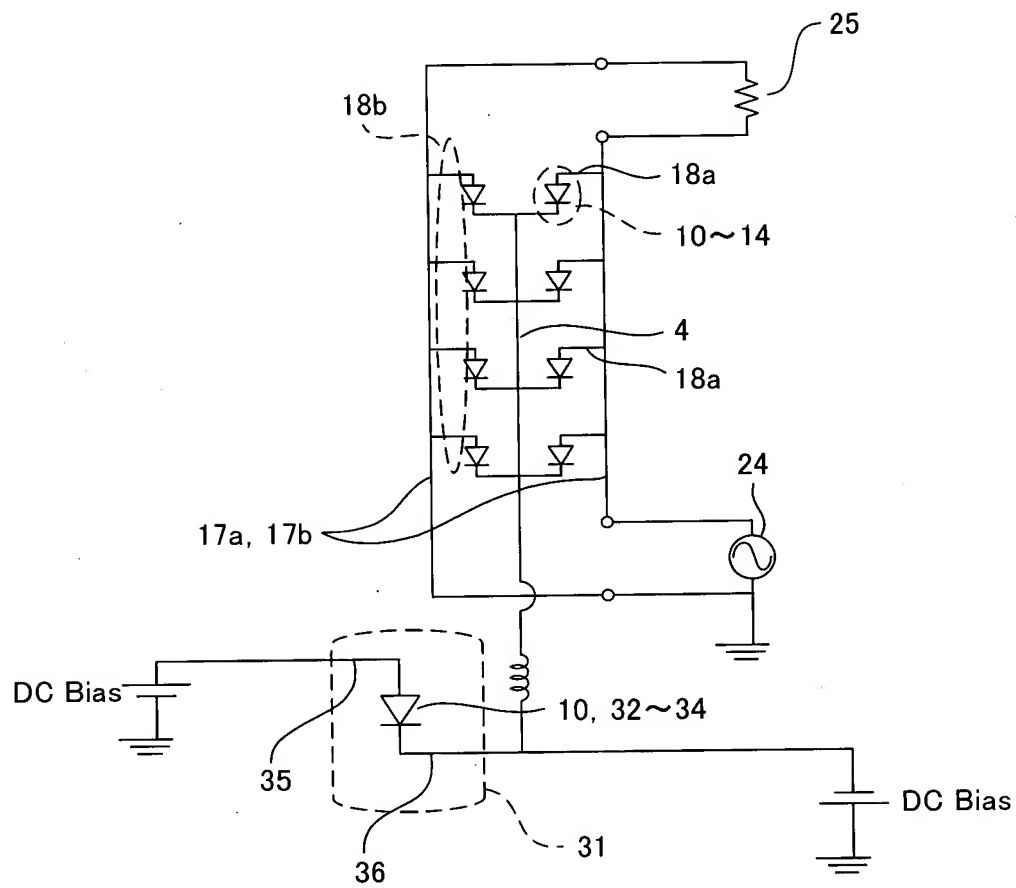




FIG. 30



11

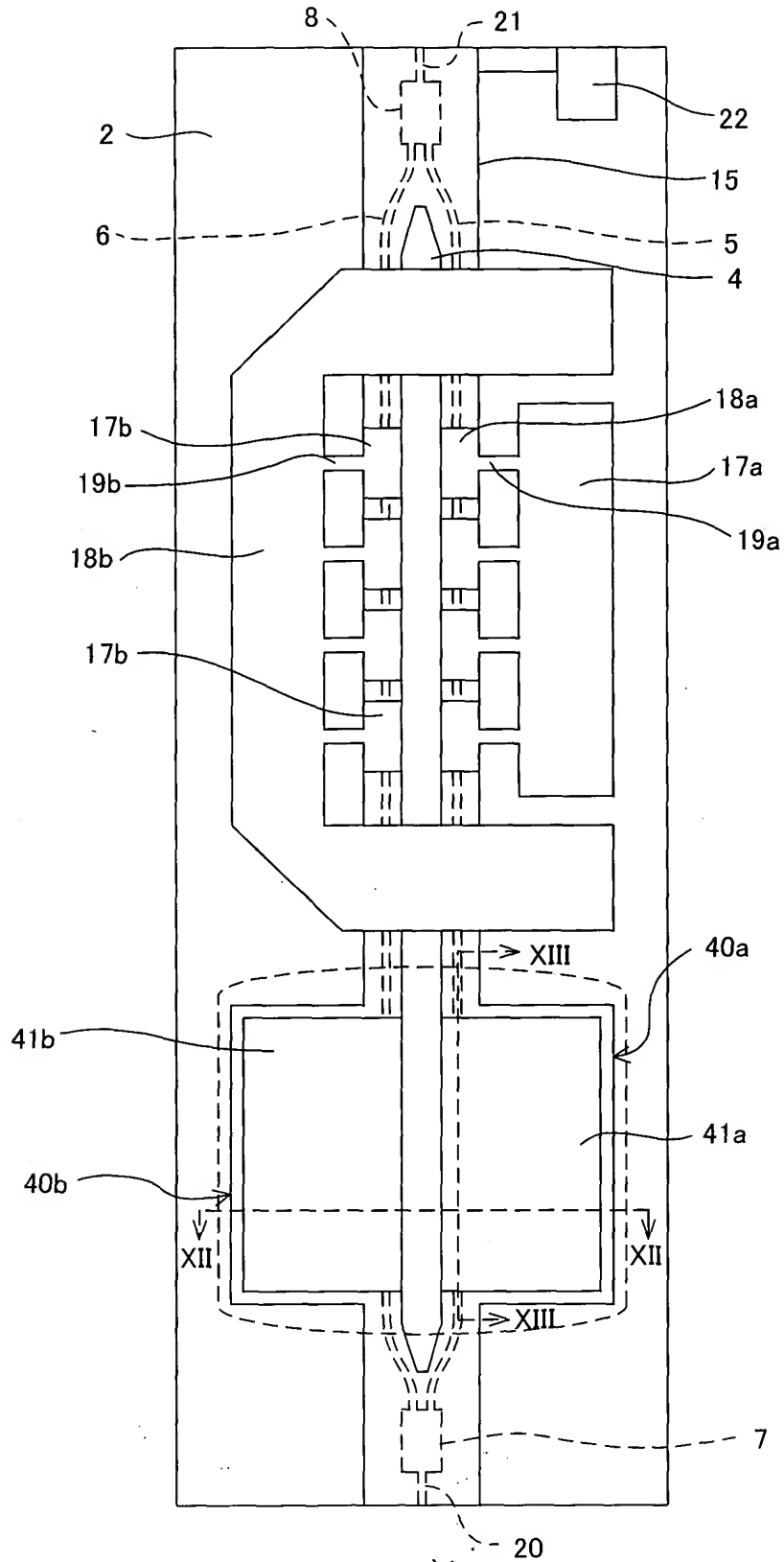


FIG. 32

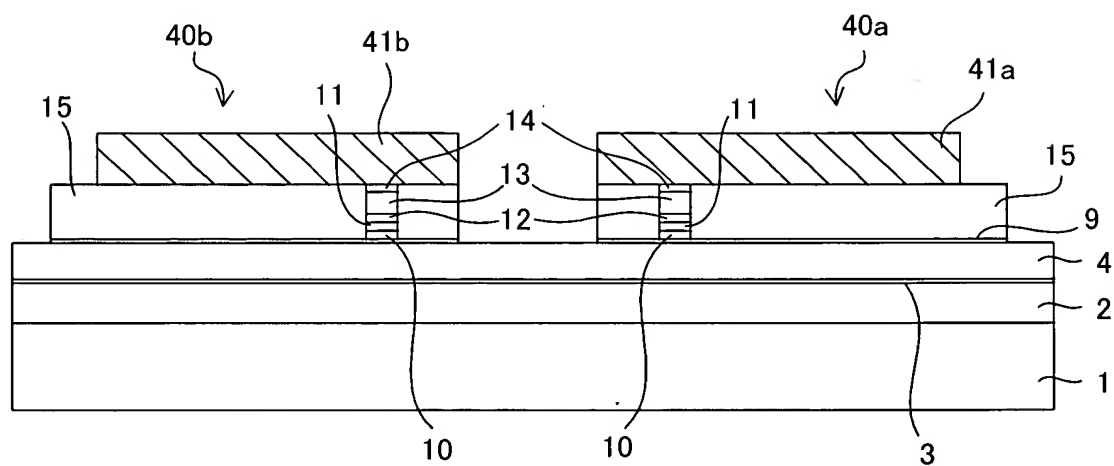


FIG. 33

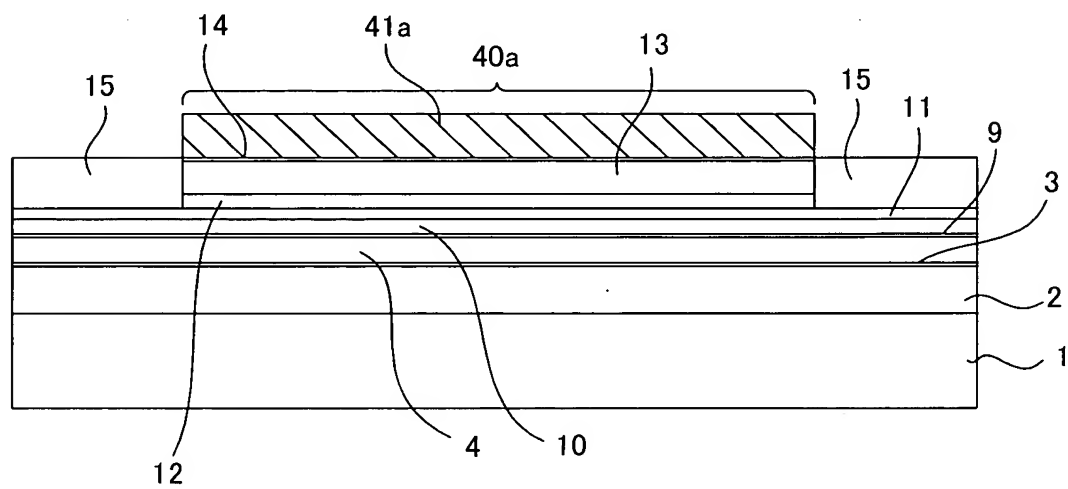
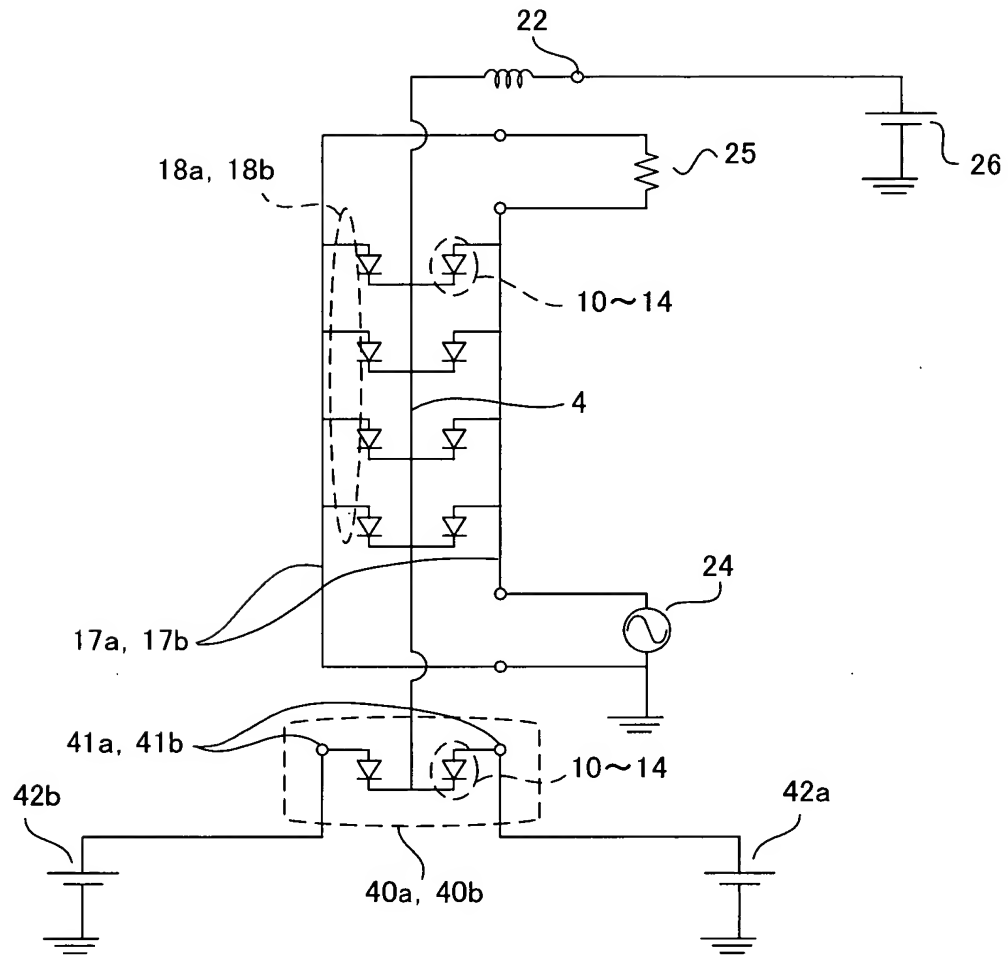
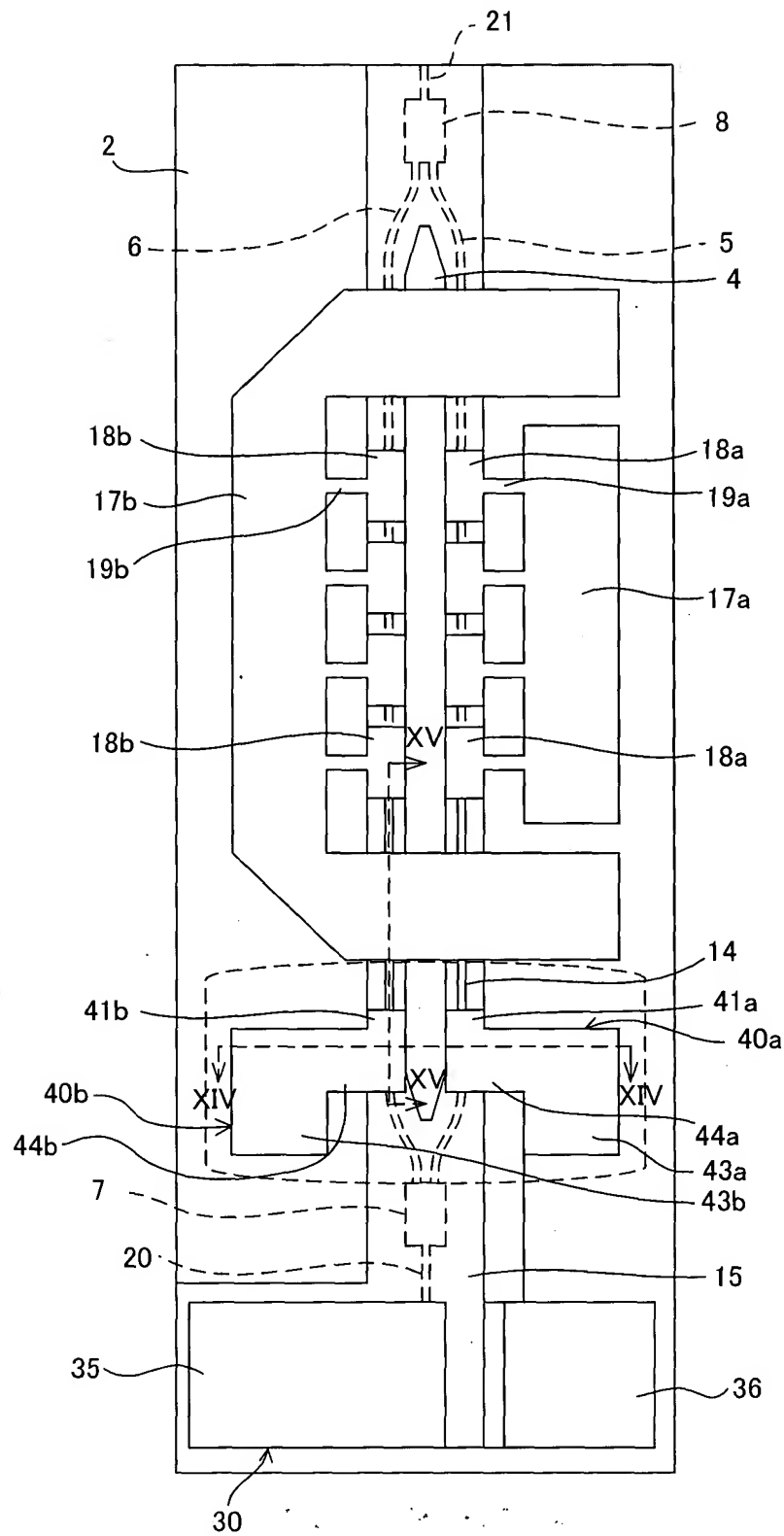


FIG. 34



# FIG. 35



This cross-sectional view shows a semiconductor device with two transistors. The device is built on a substrate 1, with a gate stack 2. A gate electrode 3 is positioned between the two transistors. The first transistor (40a) has a gate stack 4, a gate electrode 15, a channel region 5, a source/drain region 10, and a contact 11. The second transistor (40b) has a gate stack 6, a gate electrode 14, a channel region 9, a source/drain region 10, and a contact 11. The device also includes a passivation layer 12, a protective layer 13, and a top layer 14. The gate stack 4 is formed by a gate oxide 41a and a gate electrode 43a. The gate stack 6 is formed by a gate oxide 41b and a gate electrode 43b. The source/drain regions 10 are formed by a source/drain oxide 44a and a source/drain electrode 44b. The contacts 11 are formed by a contact oxide 44a and a contact electrode 44b.

FIG. 37

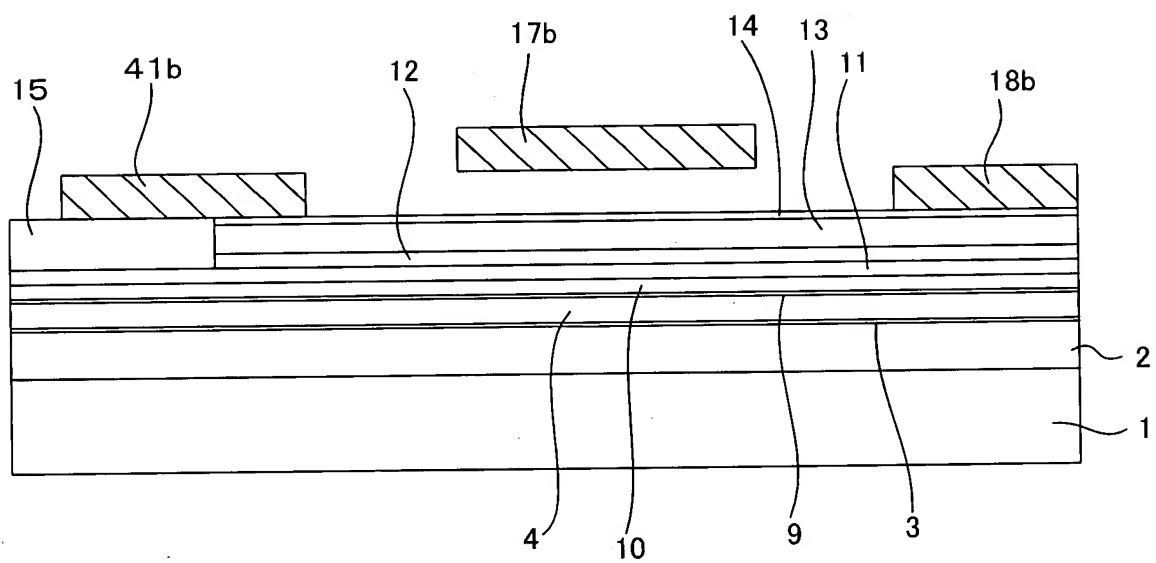


FIG. 38

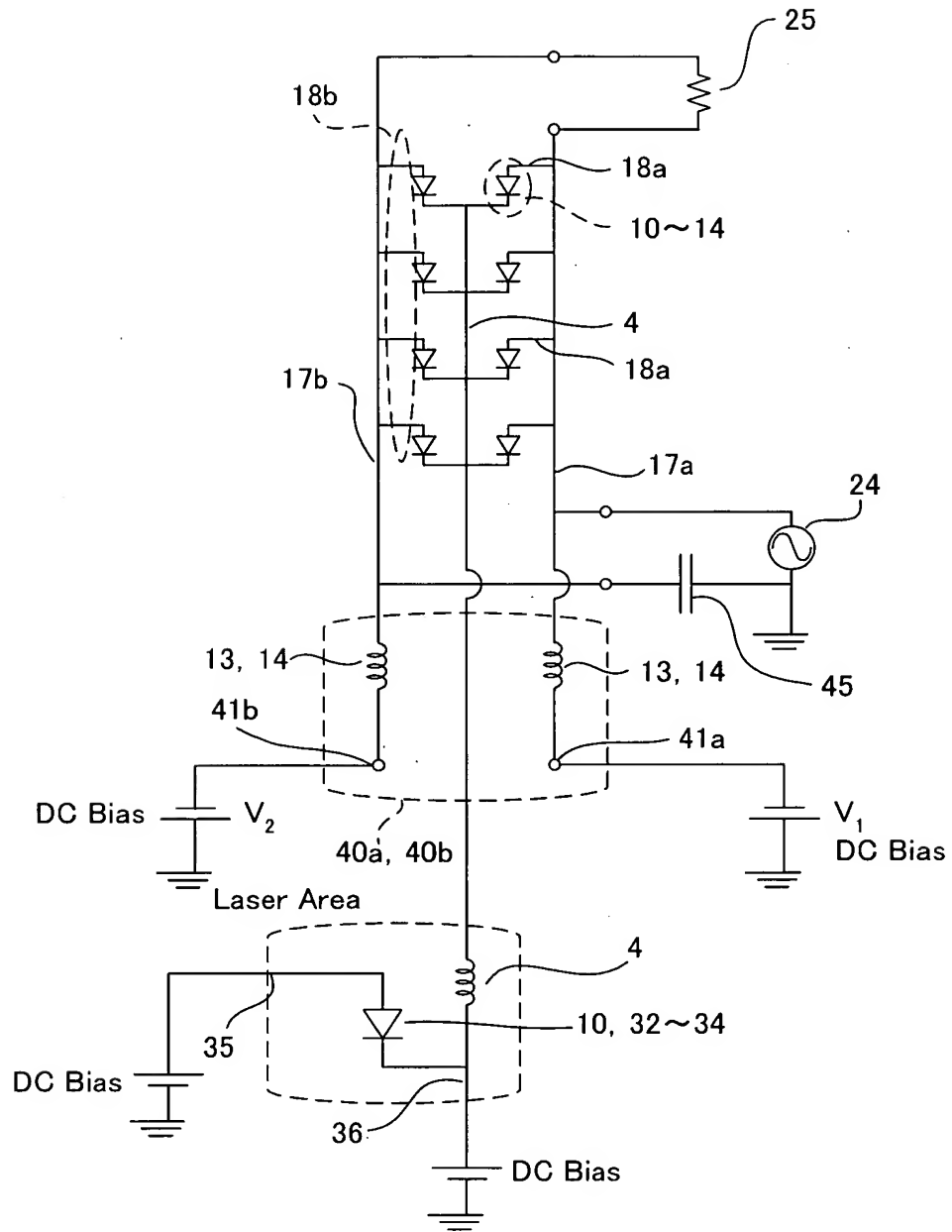




FIG. 39

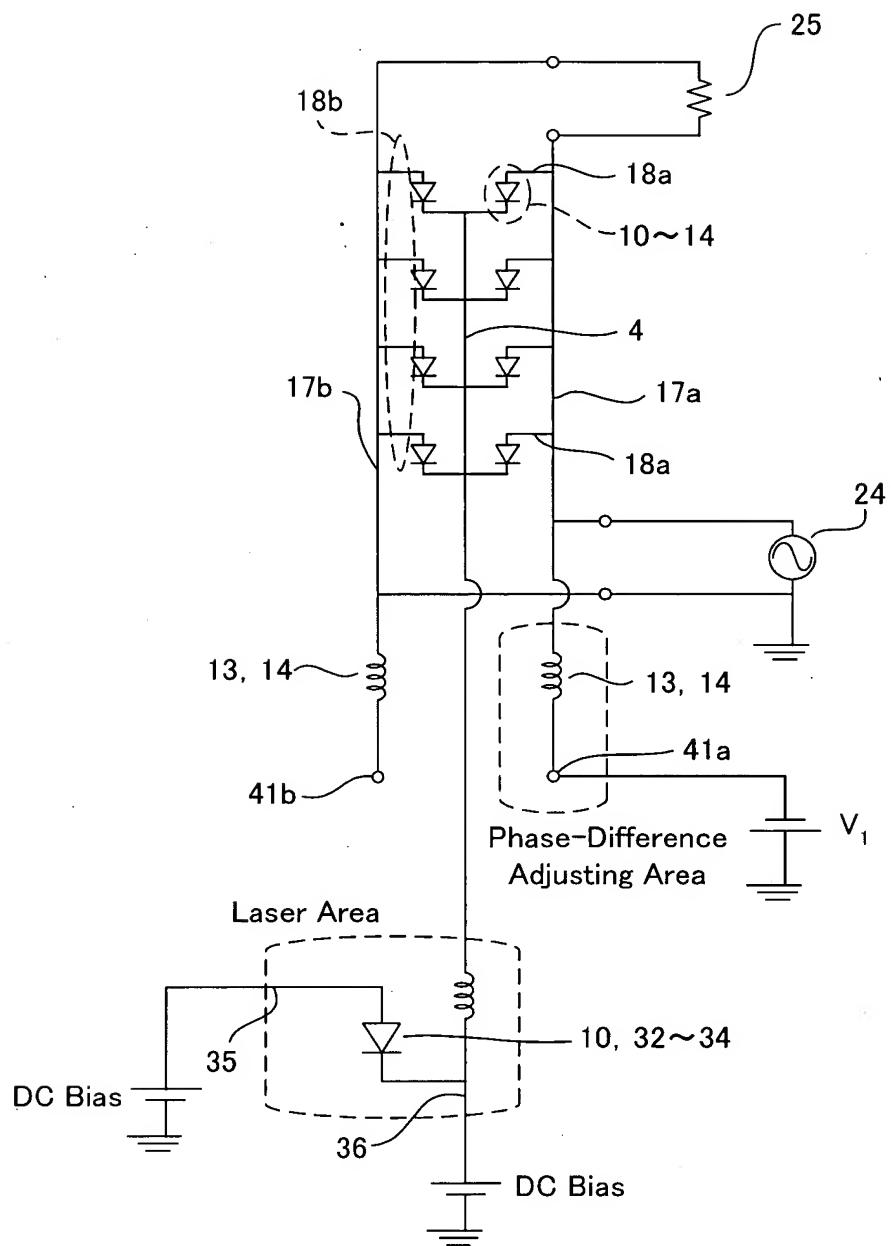


FIG. 40

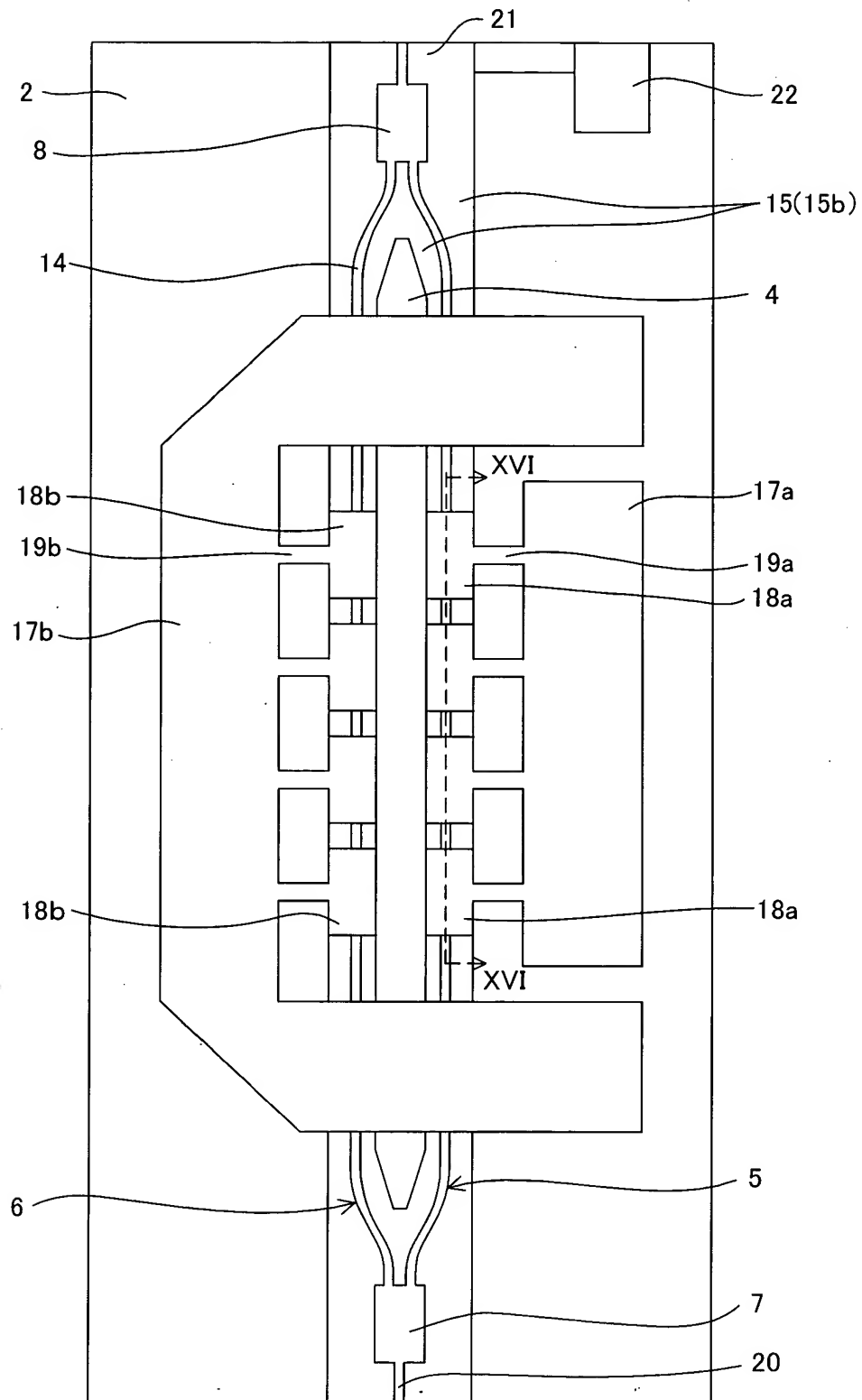


FIG. 41

